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(71) Applicant *(for all designated States except US)*: NORTH CAROLINA STATE UNIVERSITY [US/US]; Holladay Hall, Campus Box 7003, Raleigh, NC 27695–7003 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: ZHELEVA, Tsvetanka [BG/US]; 2109 Copeland Way, Chapel Hill, NC 27514 (US). THOMSON, Darren, B. [US/US]; 312–D Bargate Drive, Cary, NC 27511 (US). SMITH, Scott, A. [US/US]; 505 Crawley Run #101, Centerville, OH 45458 (US). LINTHICUM, Kevin, J. [US/US]; 474 Crosslink Drive, Angier, NC 27501 (US). GEHRKE, Thomas [DE/US]; 116B Bim Street, Carrboro, NC 27510 (US). DAVIS, Robert, F. [US/US]; 5705 Calton Drive, Raleigh, NC 27612 (US).

(74) Agents: BIGEL, Mitchell, S. et al.; Myers Bigel Sibley & Sajovec, P.A., P.O. Box 37428, Raleigh, NC 27627 (US).

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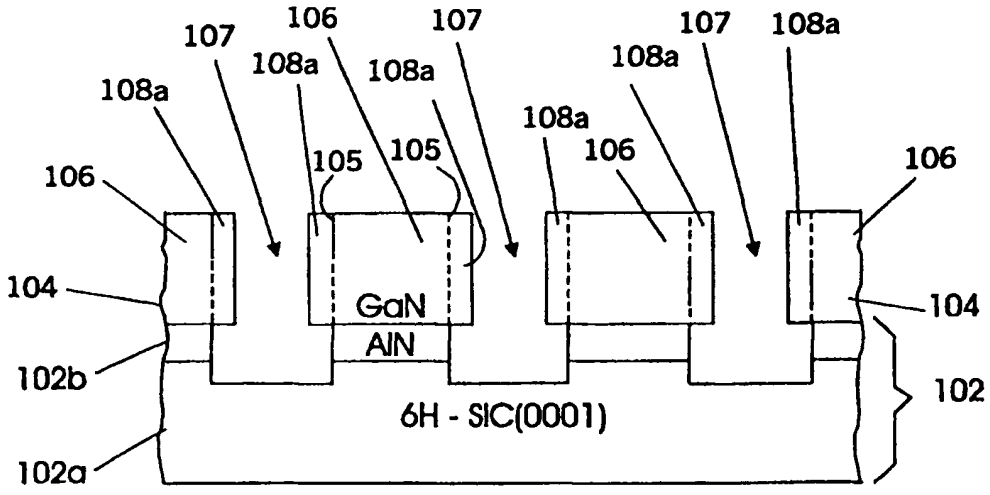

(57) Abstract

A sidewall (105) of an underlying gallium nitride layer (106) is laterally grown into a trench (107) in the underlying gallium nitride layer, to thereby form a lateral gallium nitride semiconductor layer (108a). Microelectronic devices may then be formed in the lateral gallium nitride layer. Dislocation defects do not significantly propagate laterally from the sidewall into the trench in the underlying gallium nitride layer, so that the lateral gallium nitride semiconductor layer is relatively defect free. Moreover, the sidewall growth may be accomplished without the need to mask portions of the underlying gallium nitride layer during growth of the lateral gallium nitride layer. The defect density of the lateral gallium nitride semiconductor layer may be further decreased by growing a second gallium nitride semiconductor layer from the lateral gallium nitride layer.

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FABRICATION OF GALLIUM NITRIDE SEMICONDUCTOR LAYERS BY LATERAL GROWTH FROM TRENCH SIDEWALLS

Field of the Invention

This invention relates to microelectronic devices and fabrication methods, and more particularly to gallium nitride semiconductor devices and fabrication methods therefor.

Background of the Invention

Gallium nitride is being widely investigated for microelectronic devices including but not limited to transistors, field emitters and optoelectronic devices. It will be understood that, as used herein, gallium nitride also includes alloys of gallium nitride such as aluminum gallium nitride, indium gallium nitride and aluminum indium gallium nitride.

A major problem in fabricating gallium nitride-based microelectronic devices is the fabrication of gallium nitride semiconductor layers having low defect densities. It is known that one contributor to defect density is the substrate on which the gallium nitride layer is grown. Accordingly, although gallium nitride layers have been grown on sapphire substrates, it is known to reduce defect density by growing gallium nitride layers on aluminum nitride buffer layers which are themselves formed on silicon carbide substrates. Notwithstanding these advances, continued reduction in defect density is desirable.

It is also known to fabricate gallium nitride structures through openings in a mask. For example, in fabricating field emitter arrays, it is known to selectively grow gallium nitride on stripe or circular patterned substrates. See, for example, the publications by Nam et al. entitled *"Selective Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on GaN/AlN/6H-SiC(0001) Multilayer Substrates Via Organometallic Vapor Phase Epitaxy"*, Proceedings of the Materials Research Society, December 1996, and *"Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on Patterened Substrates via Organometallic Vapor Phase Epitaxy"*, Japanese Journal of Applied Physics., Vol. 36, Part 2, No. 5A, May

1997, pp. L532-L535. As disclosed in these publications, undesired ridge growth or lateral overgrowth may occur under certain conditions.

Summary of the Invention

It is therefore an object of the present invention to provide improved methods of fabricating gallium nitride semiconductor layers, and improved gallium nitride layers so fabricated.

It is another object of the invention to provide methods of fabricating gallium nitride semiconductor layers that can have low defect densities, and gallium nitride semiconductor layers so fabricated.

These and other objects are provided, according to the present invention by laterally growing a sidewall of an underlying gallium nitride layer into a trench in the underlying gallium nitride layer, to thereby form a lateral gallium nitride layer. Microelectronic devices may then be formed in the lateral gallium nitride layer.

It has been found, according to the present invention, that dislocation defects do not significantly propagate laterally from the sidewall into the trench in the underlying gallium nitride layer, so that the lateral gallium nitride semiconductor layer is relatively defect free. The sidewall growth may be accomplished without the need to mask portions of the underlying gallium nitride layer during growth of the lateral gallium nitride layer.

According to another aspect of the present invention, a pair of sidewalls of the underlying gallium nitride layer are laterally grown into a trench in the underlying gallium nitride layer between the pair of sidewalls until the grown sidewalls coalesce in the trench. The lateral gallium nitride semiconductor layer may be laterally grown using metalorganic vapor phase epitaxy (MOVPE). For example, the lateral gallium nitride layer may be laterally grown using triethylgallium (TEG) and ammonia (NH_3) precursors at 1000-1100°C and 45 Torr. Preferably, TEG at 13-39μmol/min and NH_3 at 1500 sccm are used in combination with 3000 sccm H_2 diluent. Most preferably, TEG at 26μmol/min, NH_3 at 1500 sccm and H_2 at 3000 sccm at a temperature of 1100°C and 45 Torr are used. The underlying gallium nitride layer preferably is formed on a substrate such as 6H-SiC(0001), which itself includes a buffer layer such as aluminum nitride thereon. Other substrates such as sapphire, and other buffer

layers such as low temperature gallium nitride, may be used. Multiple substrate layers and buffer layers also may be used.

The underlying gallium nitride layer including the sidewall may be formed by forming the trench in the underlying gallium nitride layer, such that the trench includes the sidewall. Alternatively, the sidewall may be formed by forming a post on the underlying gallium nitride layer, the post including the sidewall and defining the trench. A series of alternating trenches and posts is preferably formed to form a plurality of sidewalls. Trenches and/or posts may be formed by selective etching, selective epitaxial growth, combinations of etching and growth, or other techniques. The trenches may extend into the buffer layer and into the substrate.

The sidewall of the underlying gallium nitride layer is laterally grown into the trench, to thereby form the lateral gallium nitride layer of lower defect density than the defect density of the underlying gallium nitride layer. Some vertical growth may also occur. The laterally grown gallium nitride layer is vertically grown while propagating the lower defect density. Vertical growth may also take place simultaneous with the lateral growth.

The defect density of the overgrown gallium nitride semiconductor layer may be further decreased by growing a second gallium nitride semiconductor layer from the lateral gallium nitride layer. In one embodiment, the lateral gallium nitride layer is masked with a mask that includes an array of openings therein. The lateral gallium nitride layer is grown through the array of openings and onto the mask, to thereby form an overgrown gallium nitride semiconductor layer. In another embodiment, the lateral gallium nitride layer is grown vertically. A plurality of second sidewalls are formed in the vertically grown lateral gallium nitride layer to define a plurality of second trenches. The plurality of second sidewalls of the vertically grown lateral gallium nitride layer are then laterally grown into the plurality of second trenches, to thereby form a second lateral gallium nitride layer. Microelectronic devices are then formed in the gallium nitride semiconductor layer. The plurality of sidewalls of the underlying gallium nitride layer may be grown using metalorganic vapor phase epitaxy as was described above. The second sidewalls may be grown by etching and/or selective epitaxial growth of trenches and/or posts, as was described above.

Gallium nitride semiconductor structures according to the invention comprise an underlying gallium nitride layer including a trench having a sidewall, and a lateral

gallium nitride layer that extends from the sidewall of the underlying gallium nitride layer into the trench. A vertical gallium nitride layer extends from the lateral gallium nitride layer. A plurality of microelectronic devices are included in the vertical gallium nitride layer. A series of alternating trenches and posts may be provided to define a plurality of sidewalls. The underlying gallium nitride layer includes a predetermined defect density, and the lateral gallium nitride layer is of lower defect density than the predetermined defect density.

Other embodiments of gallium nitride semiconductor structures according to the invention comprise a mask including an array of openings therein on the lateral gallium nitride layer and a vertical gallium nitride layer that extends from the lateral gallium nitride layer through the openings and onto the mask. Alternatively, a vertical gallium nitride layer extends from the lateral gallium nitride layer and includes a plurality of second sidewalls therein. A second lateral gallium nitride layer extends from the plurality of second sidewalls. Microelectronic devices are included in the second lateral gallium nitride layer. Accordingly, low defect density gallium nitride semiconductor layers may be produced, to thereby allow the production of high performance microelectronic devices.

Brief Description of the Drawings

Figures 1-5 are cross-sectional views of first embodiments of gallium nitride semiconductor structures during intermediate fabrication steps according to the present invention.

Figures 6-10 are cross-sectional views of second embodiments of gallium nitride semiconductor structures during intermediate fabrication steps according to the present invention.

Figures 11-15 are cross-sectional views of third embodiments of gallium nitride semiconductor structures during intermediate fabrication steps according to the present invention.

Detailed Description of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different

forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or "onto" another element, it can be directly on the other element or intervening elements may also be present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Referring now to Figures 1-5, methods of fabricating gallium nitride semiconductor structures according to a first embodiment of the present invention will now be described. As shown in Figure 1, an underlying gallium nitride layer **104** is grown on a substrate **102**. The substrate **102** may include a 6H-SiC(0001) substrate **102a** and an aluminum nitride buffer layer **102b**. The crystallographic designation conventions used herein are well known to those having skill in the art, and need not be described further. The gallium nitride layer **104** may be between 1.0 and 2.0μm thick, and may be grown at 1000°C on a high temperature (1100°C) aluminum nitride buffer layer **102b** that was deposited on the 6H-SiC substrate **102a** in a cold wall vertical and inductively heated metalorganic vapor phase epitaxy system using triethylgallium at 26μmol/min, ammonia at 1500 sccm and 3000 sccm hydrogen diluent. Additional details of this growth technique may be found in a publication by T.W. Weeks et al. entitled *"GaN Thin Films Deposited Via Organometallic Vapor Phase Epitaxy on α(6H)-SiC(0001) Using High-Temperature Monocrystalline AlN Buffer Layers"*, Applied Physics Letters, Vol. 67, No. 3, July 17, 1995, pp. 401-403, the disclosure of which is hereby incorporated herein by reference. Other substrates, with or without buffer layers, may be used.

Still referring to Figure 1, the underlying gallium nitride layer **104** includes a plurality of sidewalls **105** therein. It will be understood by those having skill in the art that the sidewalls **105** may be thought of as being defined by a plurality of spaced apart posts **106**, that also may be referred to as "mesas", "pedestals" or "columns". The sidewalls **105** may also be thought of as being defined by a plurality of trenches **107**, also referred to as "wells" in the underlying gallium nitride layer **104**. The sidewalls **105** may also be thought of as being defined by a series of alternating

trenches **107** and posts **106**. It will be understood that the posts **106** and the trenches **107** that define the sidewalls **105** may be fabricated by selective etching and/or selective epitaxial growth and/or other conventional techniques. Moreover, it will also be understood that the sidewalls need not be orthogonal to the substrate **102**, but rather may be oblique thereto. Finally, it will also be understood that although the sidewalls **105** are shown in cross-section in Figure 1, the posts **106** and trenches **107** may define elongated regions that are straight, V-shaped or have other shapes. As shown in Figure 1, the trenches **107** may extend into the buffer layer **102b** and into the substrate **102a**, so that subsequent gallium nitride growth occurs preferentially on the sidewalls **105** rather than on the trench floors. In other embodiments, the trenches may not extend into the substrate **102a**, and also may not extend into buffer layer **102b**, depending, for example, on the trench geometry and the lateral versus vertical growth rates of the gallium nitride.

Referring now to Figure 2, the sidewalls **105** of the underlying gallium nitride layer **104** are laterally grown to form a lateral gallium nitride layer **108a** in the trenches **107**. Lateral growth of gallium nitride may be obtained at 1000-1100°C and 45 Torr. The precursors TEG at 13-39μmol/min and NH_3 at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. As used herein, the term "lateral" means a direction that is orthogonal to the sidewalls **105**. It will also be understood that some vertical growth on the posts **106** may also take place during the lateral growth from sidewalls **105**. As used herein, the term "vertical" denotes a directional parallel to the sidewalls **105**.

Referring now to Figure 3, continued growth of the lateral gallium nitride layer **108a** causes vertical growth onto the underlying gallium nitride layer **104**, specifically onto the posts **106**, to form a vertical gallium nitride layer **108b**. Growth conditions for vertical growth may be maintained as was described in connection with Figure 2. As also shown in Figure 3, continued vertical growth into trenches **107** may take place at the bottom of the trenches.

Referring now to Figure 4, growth is allowed to continue until the lateral growth fronts coalesce in the trenches **107** at the interfaces **108c**, to form a continuous gallium nitride semiconductor layer in the trenches. The total growth time may be approximately 60 minutes. As shown in Figure 5, microelectronic devices **110** may

then be formed in the lateral gallium nitride semiconductor layer **108a**. Devices may also be formed in vertical gallium nitride layer **108b**.

Accordingly, in Figure 5, gallium nitride semiconductor structures **100** according to a first embodiment of the present invention are illustrated. The gallium nitride structures **100** include the substrate **102**. The substrate may be sapphire or gallium nitride or other conventional substrates. However, preferably, the substrate includes the 6H-SiC(0001) substrate **102a** and the aluminum nitride buffer layer **102b** on the silicon carbide substrate **102a**. The aluminum nitride buffer layer **102b** may be 0.1μm thick.

The fabrication of the substrate **102** is well known to those having skill in the art and need not be described further. Fabrication of silicon carbide substrates are described, for example, in U.S. Patents 4,865,685 to Palmour; Re 34,861 to Davis et al.; 4,912,064 to Kong et al. and 4,946,547 to Palmour et al., the disclosures of which are hereby incorporated herein by reference.

The underlying gallium nitride layer **104** is also included on the buffer layer **102b** opposite the substrate **102a**. The underlying gallium nitride layer **104** may be between about 1.0 and 2.0μm thick, and may be formed using metalorganic vapor phase epitaxy (MOVPE). The underlying gallium nitride layer generally has an undesired relatively high defect density. For example, dislocation densities of between about 10^8 and $10^{10}cm^{-2}$ may be present in the underlying gallium nitride layer. These high defect densities may result from mismatches in lattice parameters between the buffer layer **102b** and the underlying gallium nitride layer **104**, and/or other causes. These high defect densities may impact the performance of microelectronic devices formed in the underlying gallium nitride layer **104**.

Still continuing with the description of Figure 5, the underlying gallium nitride layer **104** includes the plurality of sidewalls **105** that may be defined by the plurality of pedestals **106** and/or the plurality of trenches **107**. As was described above, the sidewalls may be oblique and of various elongated shapes.

Continuing with the description of Figure 5, the lateral gallium nitride layer **108a** extends from the plurality of sidewalls **105** of the underlying gallium nitride layer **104**. The lateral gallium nitride layer **108a** may be formed using metalorganic vapor phase epitaxy at about 1000-1100°C and 45 Torr. Precursors of triethygallium (TEG) at 13-39μmol/min and ammonia (NH_3) at 1500 sccm may be used in

combination with a 3000 sccm H_2 diluent, to form the lateral gallium nitride layer **108a**.

Still continuing with the description of Figure 5, the gallium nitride semiconductor structure **100** also includes the vertical gallium nitride layer **108b** that extends vertically from the posts **106**.

As shown in Figure 5, the lateral gallium nitride layer **108a** coalesces at the interfaces **108c** to form a continuous lateral gallium nitride semiconductor layer **108a** in the trenches. It has been found that the dislocation densities in the underlying gallium nitride layer **104** generally do not propagate laterally from the sidewalls **105** with the same density as vertically from the underlying gallium nitride layer **104**. Thus, the lateral gallium nitride layer **108a** can have a relatively low defect density, for example less that 10^4 cm^{-2}. Accordingly, the lateral gallium nitride layer **108b** may form device quality gallium nitride semiconductor material. Thus, as shown in Figure 5, microelectronic devices **110** may be formed in the lateral gallium nitride semiconductor layer **108a**. It will also be understood that a mask need not be used to fabricate the gallium nitride semiconductor structures **100** of Figure 5, because lateral growth is directed from the sidewalls **105**.

Referring now to Figures 6-10, second embodiments of gallium nitride semiconductor structures and fabrication methods according to the present invention will now be described. First, gallium nitride semiconductor structures of Figure 4 are fabricated as was already described with regard to Figures 1-4. Then, referring to Figure 6, the posts **106** are masked with a mask **206** that includes an array of openings therein. The mask may comprise silicon dioxide at thickness of 1000Å and may be deposited using low pressure chemical vapor deposition at 410°C. Other masking materials may be used. The mask may be patterned using standard photolithography techniques and etched in a buffered HF solution. In one embodiment, the openings are 3μm-wide openings that extend in parallel at distances of between 3 and 40μm and that are oriented along the $<1\bar{1}00>$ direction on the lateral gallium nitride layer **108a**. Prior to further processing, the structure may be dipped in a 50% hydrochloric acid (HCl) solution to remove surface oxides. It will be understood that although the mask **206** is preferably located above the posts **106**, it can also be offset therefrom.

Referring now to Figure 7, the lateral gallium nitride semiconductor layer **108a** is grown through the array of openings to form a vertical gallium nitride layer

208a in the openings. Growth of gallium nitride may be obtained, as was described in connection with Figure 2.

It will be understood that growth in two dimensions may be used to form an overgrown gallium nitride semiconductor layer. Specifically, the mask **206** may be patterned to include an array of openings that extend along two orthogonal directions such as $<1\bar{1}00>$ and $<11\bar{2}0>$. Thus, the openings can form a rectangle of orthogonal striped patterns. In this case, the ratio of the edges of the rectangle is preferably proportional to the ratio of the growth rates of the $\{11\bar{2}0\}$ and $\{1\bar{1}01\}$ facets, for example, in a ratio of 1.4:1. The openings can be equitriangular with respect to directions such as $<1\bar{1}00>$ and $<11\bar{2}0>$.

Referring now to Figure 8, continued growth of the vertical gallium nitride layer **208a** causes lateral growth onto the mask **206**, to form a second lateral gallium nitride layer **208b**. Conditions for overgrowth may be maintained as was described in connection with Figure 7.

Referring now to Figure 9, lateral overgrowth is allowed to continue until the lateral growth fronts coalesce at the second interfaces **208c** on the mask **206** to form a continuous overgrown gallium nitride semiconductor layer **208**. The total growth time may be approximately sixty minutes. As shown in Figure 10, microelectronic devices **210** may then be formed in the second lateral gallium nitride layer **208b**. The microelectronic devices may also be formed in the vertical gallium nitride layer **208a**.

Accordingly, by providing the second lateral growth layer **208b**, defects that were present in continuous gallium nitride semiconductor layer **108** may be reduced even further, to obtain device quality gallium nitride in the gallium nitride semiconductor structure **200**.

Referring now to Figures 11-15, third embodiments of gallium nitride semiconductor structures and fabrication methods according to the present invention will now be described. First, gallium nitride semiconductor structures of Figure 4 are fabricated as was already described in connection with Figures 1-4. Then, a plurality of second sidewalls **305** are formed. The second sidewalls **305** may be formed by selective epitaxial growth of second posts **306** by etching second trenches **307** in the first posts **106** and/or combinations thereof. As was already described, the second sidewalls **305** need not be orthogonal to substrate **102**, but rather may be oblique. The

second trenches **307** need not be directly over the first posts **106**, but may be laterally offset therefrom. The second trenches are preferably deep so that lateral growth preferentially occurs on the sidewalls **305** rather than on the bottom of second trenches **306**.

Referring now to Figure 12, the second sidewalls **305** of the second posts **306** and/or the second trenches **307** are laterally grown to form a second lateral gallium nitride layer **308a** in the second trenches **307**. As was already described, lateral growth of gallium nitride may be obtained at 1000-1100°C and 45 Torr. The precursors TEG at 13-39μmol/min and NH_3 at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. It will also be understood that some vertical growth may take place on the second posts **306** during the lateral growth from the second sidewalls **305**.

Referring now to Figure 13, continued growth of the second lateral gallium nitride layer **308a** causes vertical growth onto the second posts **306**, to form a second vertical gallium nitride layer **308b**. As also shown, vertical growth from the floors of the second trenches and from the tops of the second posts may also take place. Growth conditions for vertical growth may be maintained as was described in connection with Figure 12.

Referring now to Figure 14, growth is allowed to continue until the lateral growth fronts coalesce in the second trenches **307** at the second interfaces **308c** to form a second continuous gallium nitride semiconductor layer **308**. The total growth time may be approximately sixty minutes. As shown in Figure 15, microelectronic devices **310** may then be formed in the second continuous gallium nitride semiconductor layer **308**.

Accordingly, third embodiments of gallium nitride semiconductor structures **300** according to the present invention may be formed without the need to mask gallium nitride for purposes of defining lateral growth. Rather, lateral growth from first and second sidewalls may be used. By performing two separate lateral growths, the defect density may be reduced considerably.

Additional discussion of methods and structures of the present invention will now be provided. The first and second trenches **107** and **307** and the openings in the mask **206** are preferably rectangular trenches and openings that preferably extend

along the $<11\bar{2}0>$ and/or $<1\bar{1}00>$ directions on the underlying gallium nitride layer **104** or the first lateral gallium nitride layer **108a**. Truncated triangular stripes having $(1\bar{1}01)$ slant facets and a narrow (0001) top facet may be obtained for trenches and/or mask openings along the $<11\bar{2}0>$ direction. Rectangular stripes having a (0001) top facet, $(11\bar{2}0)$ vertical side faces and $(1\bar{1}01)$ slant facets may be grown along the $<1\bar{1}00>$ direction. For growth times up to 3 minutes, similar morphologies may be obtained regardless of orientation. The stripes develop into different shapes if the growth is continued.

The amount of lateral growth generally exhibits a strong dependence on trench and/or mask opening orientation. The lateral growth rate of the $<1\bar{1}00>$ oriented trenches and/or mask openings is generally much faster than those along $<11\bar{2}0>$. Accordingly, it is most preferred to orient the trenches and/or mask openings, so that they extend along the $<1\bar{1}00>$ direction of the underlying gallium nitride layer **104** or the first lateral gallium nitride layer **108a**.

The different morphological development as a function of trench and/or mask opening orientation appears to be related to the stability of the crystallographic planes in the gallium nitride structure. Trenches and/or mask openings oriented along $<11\bar{2}0>$ may have wide $(1\bar{1}00)$ slant facets and either a very narrow or no (0001) top facet depending on the growth conditions. This may be because $(1\bar{1}01)$ is the most stable plane in the gallium nitride wurtzite crystal structure, and the growth rate of this plane is lower than that of others. The $\{1\bar{1}01\}$ planes of the $<1\bar{1}00>$ oriented trenches and/or mask openings may be wavy, which implies the existence of more than one Miller index. It appears that competitive growth of selected $\{1\bar{1}01\}$ planes occurs during the deposition which causes these planes to become unstable and which causes their growth rate to increase relative to that of the $(1\bar{1}01)$ of trenches and/or mask openings oriented along $<11\bar{2}0>$.

The morphologies of the gallium nitride layers selectively grown from trenches and/or mask openings oriented along $<1\bar{1}00>$ are also generally a strong function of the growth temperatures. Layers grown at 1000°C may possess a truncated triangular shape. This morphology may gradually change to a rectangular cross-section as the growth temperature is increased. This shape change may occur as a

result of the increase in the diffusion coefficient and therefore the flux of the gallium species along the (0001) top plane onto the $\{1\bar{1}01\}$ planes with an increase in growth temperature. This may result in a decrease in the growth rate of the (0001) plane and an increase in that of the $\{1\bar{1}01\}$. This phenomenon has also been observed in the selective growth of gallium arsenide on silicon dioxide. Accordingly, temperatures of 1100°C appear to be most preferred.

The morphological development of the gallium nitride regions also appears to depend on the flow rate of the TEG. An increase in the supply of TEG generally increases the growth rate in both the lateral and the vertical directions. However, the lateral/vertical growth rate ratio decrease from 1.7 at the TEG flow rate of 13μmol/min to 0.86 at 39μmol.min. This increased influence on growth rate along <0001> relative to that of $<11\bar{2}0>$ with TEG flow rate may be related to the type of reactor employed, wherein the reactant gases flow vertically and perpendicular to the substrate. The considerable increase in the concentration of the gallium species on the surface may sufficiently impede their diffusion to the $\{1\bar{1}01\}$ planes such that chemisorption and gallium nitride growth occur more readily on the (0001) plane.

Continuous 2μm thick gallium nitride semiconductor layers may be obtained using 3μm wide trenches and/or mask openings spaced 7μm apart and oriented along $<1\bar{1}00>$, at 1100°C and a TEG flow rate of 26μmol/min. The continuous gallium nitride semiconductor layers may include subsurface voids that form when two growth fronts coalesce. These voids may occur most often using lateral growth conditions wherein rectangular trenches and/or mask openings having vertical $\{11\bar{2}0\}$ side facets developed.

The continuous gallium nitride semiconductor layers may have a microscopically flat and pit-free surface. The surfaces of the laterally grown gallium nitride layers may include a terrace structure having an average step height of 0.32nm. This terrace structure may be related to the laterally grown gallium nitride, because it is generally not included in much larger area films grown only on aluminum nitride buffer layers. The average RMS roughness values may be similar to the values obtained for the underlying gallium nitride layer **104**.

Threading dislocations, originating from the interface between the underlying gallium nitride layer **104** and the buffer layer **102b**, appear to propagate to the top

surface of the underlying gallium nitride layer **104**. The dislocation density within these regions is approximately 10^9 cm^{-2}. By contrast, threading dislocations do not appear to readily propagate laterally. Rather, the lateral gallium nitride regions **108a** and **308a** contain only a few dislocations. These few dislocations may be formed parallel to the (0001) plane via the extension of the vertical threading dislocations after a 90° bend in the regrown region. These dislocations do not appear to propagate to the top surface of the overgrown gallium nitride layer.

As described, the formation mechanism of the selectively grown gallium nitride layers is lateral epitaxy. The two main stages of this mechanism are vertical growth and lateral growth. During vertical growth through a mask, the deposited gallium nitride grows selectively within the mask openings more rapidly than it grows on the mask, apparently due to the much higher sticking coefficient, s, of the gallium atoms on the gallium nitride surface (s=1) compared to on the mask (s<<1). Since the SiO_2 bond strength is 799.6 kJ/mole and much higher than that of Si-N (439 kJ/mole), Ga-N (103 kJ/mole), and Ga-O (353.6 kJ/mole), Ga or N atoms should not readily bond to the mask surface in numbers and for a time sufficient to cause gallium nitride nuclei to form. They would either evaporate or diffuse along the mask surface to the opening in the mask or to the vertical gallium nitride surfaces which have emerged. During lateral growth, the gallium nitride grows simultaneously both vertically and laterally.

Surface diffusion of gallium and nitrogen on the gallium nitride may play a role in gallium nitride selective growth. The major source of material appears to be derived from the gas phase. This may be demonstrated by the fact that an increase in the TEG flow rate causes the growth rate of the (0001) top facets to develop faster than the $(1\bar{1}01)$ side facets and thus controls the lateral growth.

The laterally grown gallium nitride bonds to the underlying mask sufficiently strongly so that it generally does not break away on cooling. However, lateral cracking within the SiO_2 mask may take place due to thermal stresses generated on cooling. The viscosity (ρ) of the SiO_2 at 1050°C is about $10^{15.5}$ poise which is one order of magnitude greater than the strain point (about $10^{14.5}$ poise) where stress relief in a bulk amorphous material occurs within approximately six hours. Thus, the SiO_2 mask may provide limited compliance on cooling. As the atomic arrangement on the amorphous SiO_2 surface is quite different from that on the GaN surface, chemical

bonding may occur only when appropriate pairs of atoms are in close proximity. Extremely small relaxations of the silicon and oxygen and gallium and nitrogen atoms on the respective surfaces and/or within the bulk of the SiO_2 may accommodate the gallium nitride and cause it to bond to the oxide. Accordingly, the embodiments of Figures 1-5 and 11-15, which need not employ a mask, may be particularly advantageous.

In conclusion, lateral epitaxial overgrowth may be obtained from sidewalls of an underlying gallium nitride layer via MOVPE. The growth may depend strongly on the sidewall orientation, growth temperature and TEG flow rate. Coalescence of overgrown gallium nitride regions to form regions with both extremely low densities of dislocations and smooth and pit-free surfaces may be achieved through 3μm wide trenches between 7μm wide posts and extending along the $<1\bar{1}00>$ direction, at 1100°C and a TEG flow rate of 26μmol/min. The lateral overgrowth of gallium nitride from sidewalls via MOVPE may be used to obtain low defect density regions for microelectronic devices, without the need to use masks.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed

1. A method of fabricating a gallium nitride semiconductor layer comprising the step of:

laterally growing a sidewall of an underlying gallium nitride layer into a trench in the underlying gallium nitride layer to thereby form a lateral gallium nitride semiconductor layer.

2. A method according to Claim 1 wherein the laterally growing step is followed by the step of forming microelectronic devices in the lateral gallium nitride semiconductor layer.

3. A method according to Claim 1 wherein the laterally growing step comprises the step of growing a pair of sidewalls of the underlying gallium nitride layer into a trench in the underlying gallium nitride layer between the pair of sidewalls until the grown pair of sidewalls coalesce in the trench.

4. A method according to Claim 1 wherein the laterally growing step comprises the step of laterally growing the sidewall of the underlying gallium nitride layer using metalorganic vapor phase epitaxy.

5. A method according to Claim 1 wherein the laterally growing step is preceded by the step of forming the underlying gallium nitride layer including the sidewall on a substrate.

6. A method according to Claim 5 wherein the forming step comprises the steps of:

forming a buffer layer on a substrate; and

forming the underlying gallium nitride layer on the buffer layer opposite the substrate.

7. A method according to Claim 5 wherein the forming step comprises the step of forming the trench in the underlying gallium nitride layer, the trench including the sidewall.

8. A method according to Claim 5 wherein the forming step comprises the step of forming a post on the underlying gallium nitride layer, the post including the sidewall and defining the trench.

9. A method according to Claim 1 wherein the underlying gallium nitride layer includes a predetermined defect density, and wherein the step of laterally growing a sidewall of an underlying gallium nitride layer into a trench in the underlying gallium nitride layer to thereby form a lateral gallium nitride layer comprises the steps of:

laterally growing the sidewall of the underlying gallium nitride layer to thereby form the lateral gallium nitride layer of lower defect density than the predetermined defect density; and

vertically growing the lateral gallium nitride layer while propagating the lower defect density.

10. A method according to Claim 1 wherein the growing step comprises the step of growing the sidewall of the underlying gallium nitride layer using metalorganic vapor phase epitaxy of triethylgallium at 13-39μmol/min and ammonia at 1500 sccm at a temperature of 1000°C-1100°C.

11. A method according to Claim 7 wherein the trench forming step comprises the step of selectively etching the underlying gallium nitride layer to form the trench that includes the sidewall.

12. A method according to Claim 8 wherein the post forming step comprises the step of selectively growing the underlying gallium nitride layer to form the post including the sidewall.

13. A gallium nitride semiconductor structure comprising:

an underlying gallium nitride layer including a trench having a sidewall; and

a lateral gallium nitride layer that extends from the sidewall of the underlying gallium nitride layer into the trench.

14. A structure according to Claim 13 further comprising:

a vertical gallium nitride layer that extends from the lateral gallium nitride layer.

15. A structure according to Claim 13 further comprising:

a plurality of microelectronic devices in the vertical gallium nitride layer.

16. A structure according to Claim 13 further comprising a substrate, and wherein the underlying gallium nitride layer is on the substrate.

17. A structure according to Claim 16 further comprising a buffer layer between the substrate and the underlying gallium nitride layer.

18. A structure according to Claim 13 wherein the trench includes a pair of the sidewalls, and wherein the lateral gallium nitride layer extends from the pair of sidewalls to define a continuous lateral gallium nitride.

19. A structure according to Claim 13 wherein the underlying gallium nitride layer includes a post thereon, the post including the sidewall and defining the trench.

20. A structure according to Claim 13 wherein the underlying gallium nitride layer includes a predetermined defect density, wherein the lateral gallium nitride layer is of lower defect density than the predetermined defect density.

21. A method of fabricating a gallium nitride semiconductor layer comprising the step of:

laterally growing a plurality of sidewalls of an underlying gallium nitride layer into a plurality of trenches in the underlying gallium nitride layer to thereby form a lateral gallium nitride layer.

22. A method according to Claim 21 wherein the laterally growing step is followed by the steps of:

masking the lateral gallium nitride layer with a mask that includes an array of openings therein; and

growing the lateral gallium nitride layer through the array of openings and onto the mask, to thereby form an overgrown gallium nitride semiconductor layer.

23. A method according to Claim 21 wherein the growing step is followed by the steps of:

vertically growing the lateral gallium nitride layer;

forming a plurality of second sidewalls in the vertically grown lateral gallium nitride layer to define a plurality of second trenches; and

laterally growing the plurality of second sidewalls of the vertically grown lateral gallium nitride layer into the plurality of second trenches, to thereby form a second lateral gallium nitride semiconductor layer.

24. A method according to Claim 22 wherein the laterally growing step is followed by the step of forming microelectronic devices in the overgrown gallium nitride semiconductor layer.

25. A method according to Claim 23 wherein the step of laterally growing the plurality of second sidewalls is followed by the step of forming microelectronic devices in the second lateral gallium nitride semiconductor layer.

26. A method according to Claim 21 wherein the laterally growing step comprises the step of growing the plurality of sidewalls of the underlying gallium nitride layer into the plurality of trenches in the underlying gallium nitride layer until the plurality of grown sidewalls coalesce in the trenches.

27. A method according to Claim 22 wherein the growing step comprises the step of growing the lateral gallium nitride layer through the array of openings and onto the mask until the grown lateral gallium nitride layer coalesces on the mask to form a continuous overgrown gallium nitride semiconductor layer.

28. A method according to Claim 23 wherein the step of laterally growing the plurality of second sidewalls comprises the step of laterally growing the plurality of second sidewalls of the vertically grown lateral gallium nitride layer into the plurality of second trenches until the plurality of laterally grown second sidewalls coalesce in the plurality of second trenches.

29. A method according to Claim 21 wherein the laterally growing step comprises the step of laterally growing the plurality of sidewalls of the underlying gallium nitride layer using metalorganic vapor phase epitaxy.

30. A method according to Claim 21 wherein the laterally growing step is preceded by the step of forming the underlying gallium nitride layer including the plurality of sidewalls on a substrate.

31. A method according to Claim 30 wherein the forming step comprises the steps of:

forming a buffer layer on a substrate; and

forming the underlying gallium nitride layer on the buffer layer opposite the substrate.

32. A method according to Claim 30 wherein the forming step comprises the step of forming the plurality of trenches in the underlying gallium nitride layer, the plurality of trenches including the plurality of sidewalls.

33. A method according to Claim 30 wherein the forming step comprises the step of forming a plurality of posts in the underlying gallium nitride layer, the plurality of posts including the plurality of sidewalls and defining the plurality of trenches.

34. A method according to Claim 21 wherein the underlying gallium nitride layer includes a predetermined defect density, and wherein the step of laterally growing a plurality of sidewalls of the underlying gallium nitride layer into the

plurality of trenches in the underlying gallium nitride layer to thereby form a lateral gallium nitride layer comprises the steps of:

laterally growing the plurality of sidewalls of the underlying gallium nitride layer into the plurality of trenches to thereby form a lateral gallium nitride semiconductor layer of lower defect density than the predetermined defect density; and

vertically growing the laterally gallium nitride layer while propagating the lower defect density.

35. A method according to Claim 21 wherein the laterally growing step comprises the step of laterally growing the plurality of sidewalls of the underlying gallium nitride layer using metalorganic vapor phase epitaxy of triethylgallium at 13-39μmol/min and ammonia at 1500 sccm at a temperature of 1000°C-1100°C.

36. A gallium nitride semiconductor structure comprising:

an underlying gallium nitride layer including a plurality of trenches have a plurality of sidewalls; and

a lateral gallium nitride layer that extends from the plurality of sidewalls of the underlying gallium nitride layer into the plurality of trenches.

37. A structure according to Claim 36 further comprising:

a mask including an array of openings therein on the lateral gallium nitride layer; and

a vertical gallium nitride layer that extends from the lateral gallium nitride layer, through the openings and onto the mask.

38. A structure according to Claim 36 further comprising:

a vertical gallium nitride layer that extends from the lateral gallium nitride layer, wherein the vertical gallium nitride layer includes a plurality of second sidewalls therein; and

a second lateral gallium nitride layer that extends from the plurality of second sidewalls.

39. A structure according to Claim 37 further comprising:

a plurality of microelectronic devices in the lateral gallium nitride layer.

40. A structure according to Claim 38 further comprising:

a plurality of microelectronic devices in the second lateral gallium nitride layer.

41. A structure according to Claim 36 further comprising a substrate, and wherein the underlying gallium nitride layer is on the substrate.

42. A structure according to Claim 41 further comprising a buffer layer between the substrate and the underlying gallium nitride layer.

43. A structure according to Claim 36 wherein the lateral gallium nitride layer extends from the plurality of sidewalls into the plurality of trenches to define a continuous lateral gallium nitride layer in the trenches.

44. A structure according to Claim 36 wherein the underlying gallium nitride layer includes a plurality of posts thereon, the plurality of posts including the plurality of sidewalls and defining the plurality of trenches.

45. A structure according to Claim 36 wherein the underlying gallium nitride layer includes a predetermined defect density and wherein the lateral gallium nitride layer is of lower defect density than the predetermined defect density.

FIG. 1

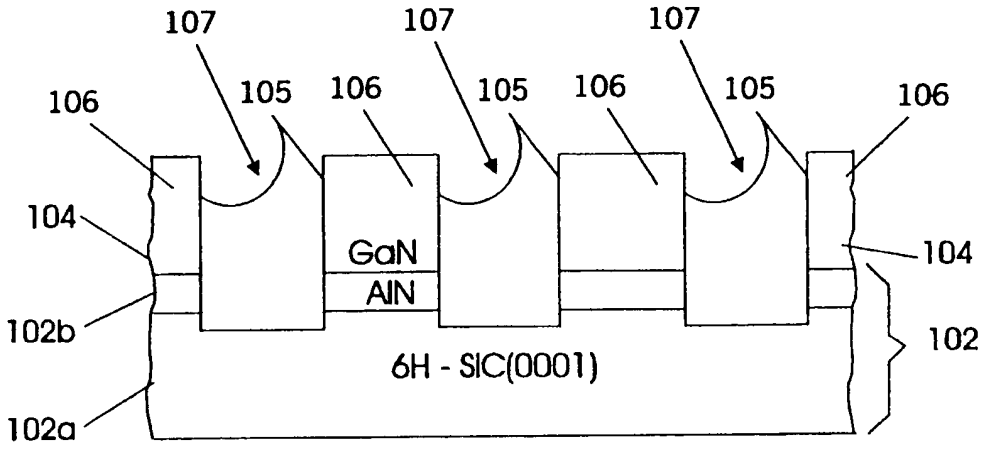
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FIG. 2

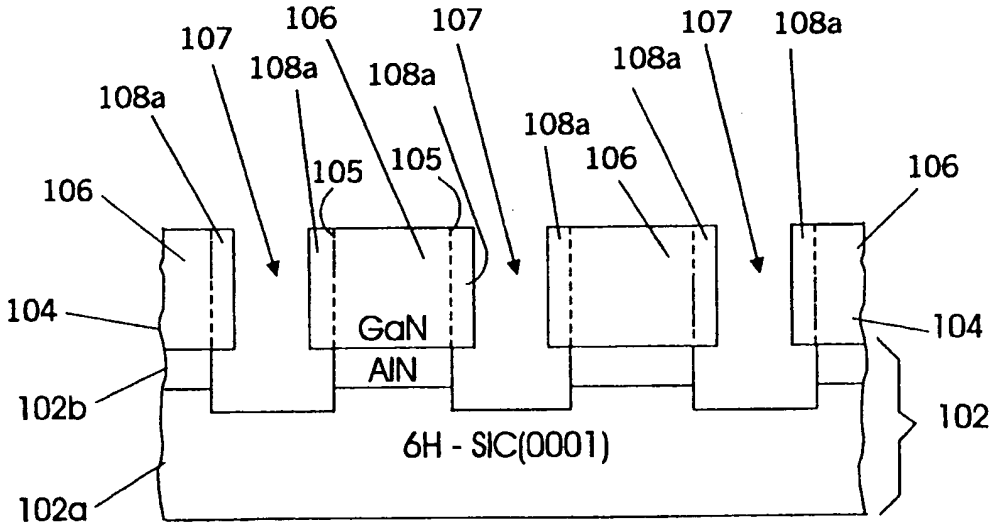
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FIG. 3

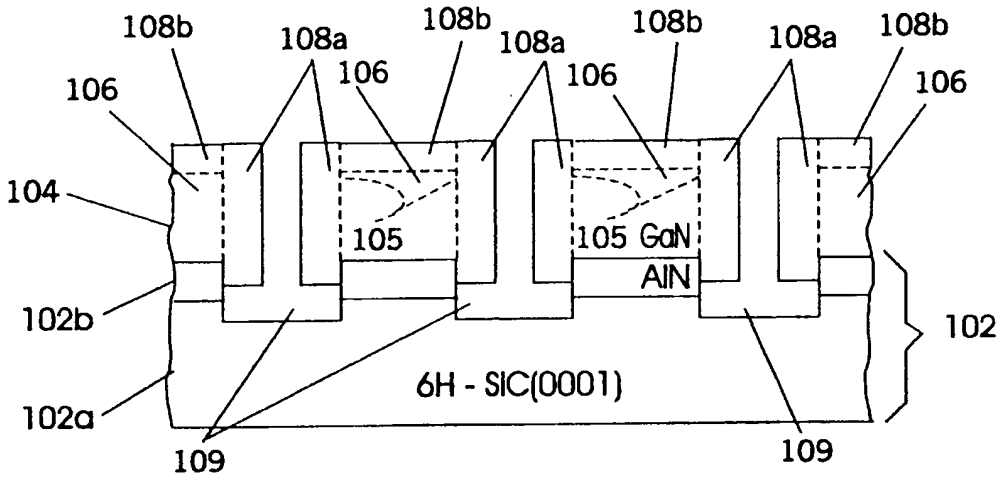
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FIG. 4

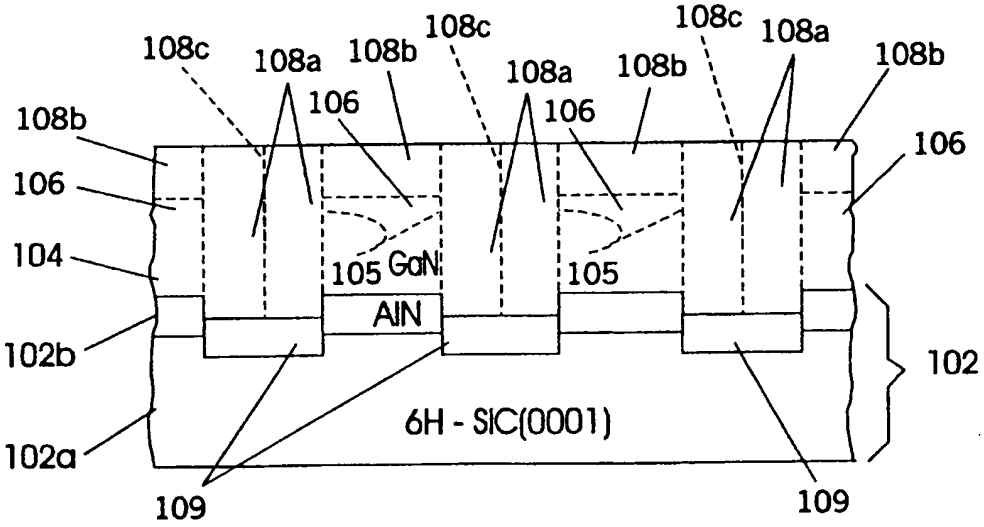
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FIG. 5

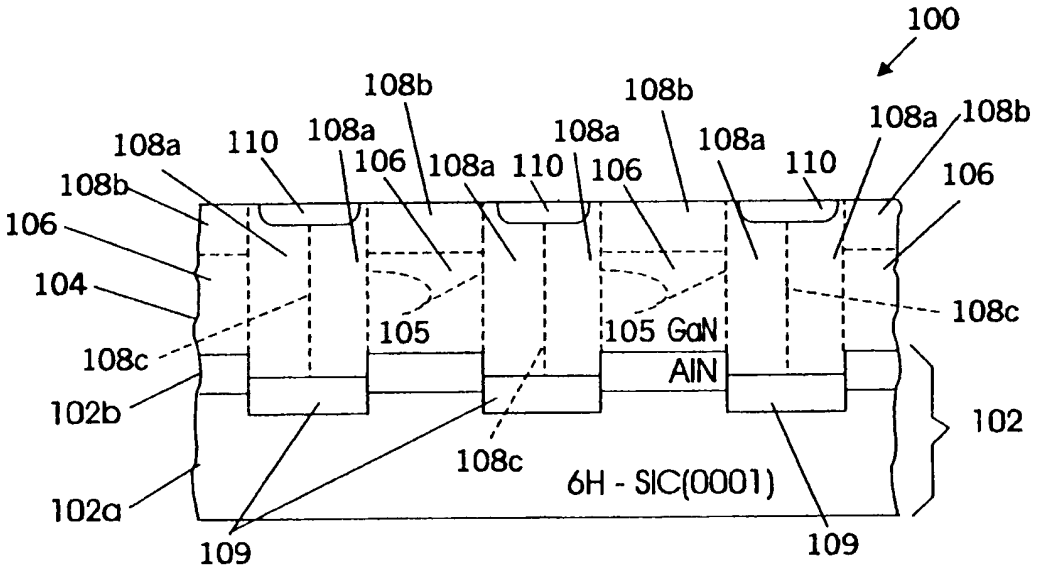
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FIG. 6

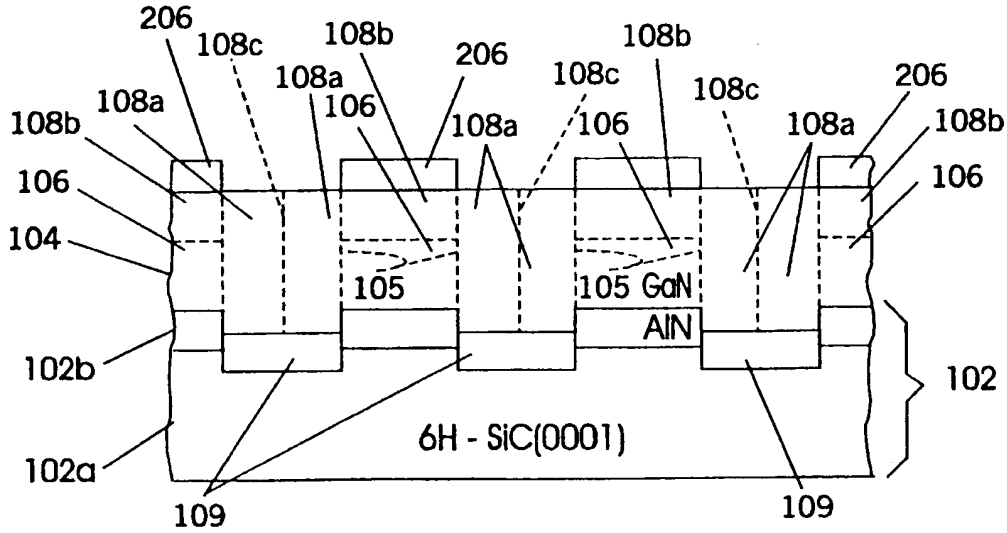
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FIG. 7

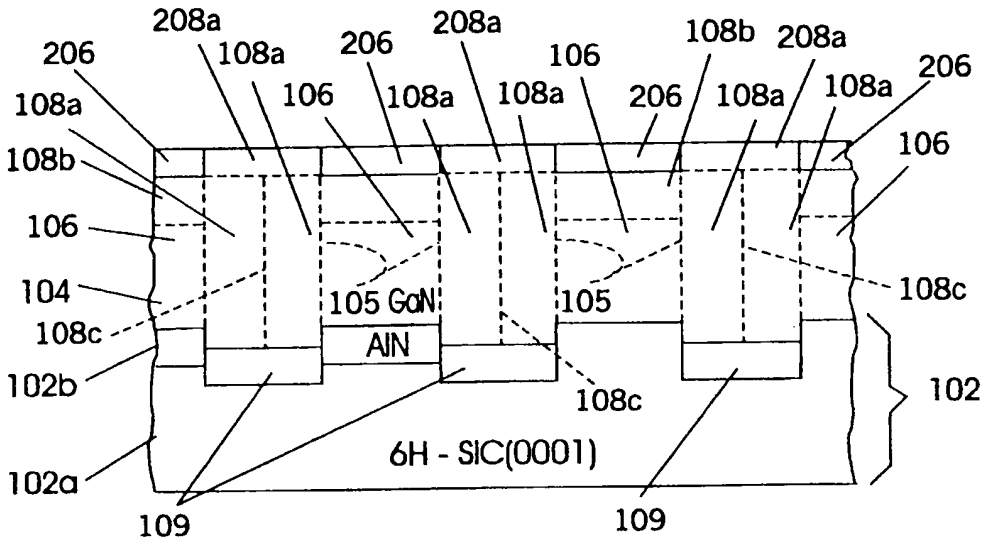
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FIG. 8

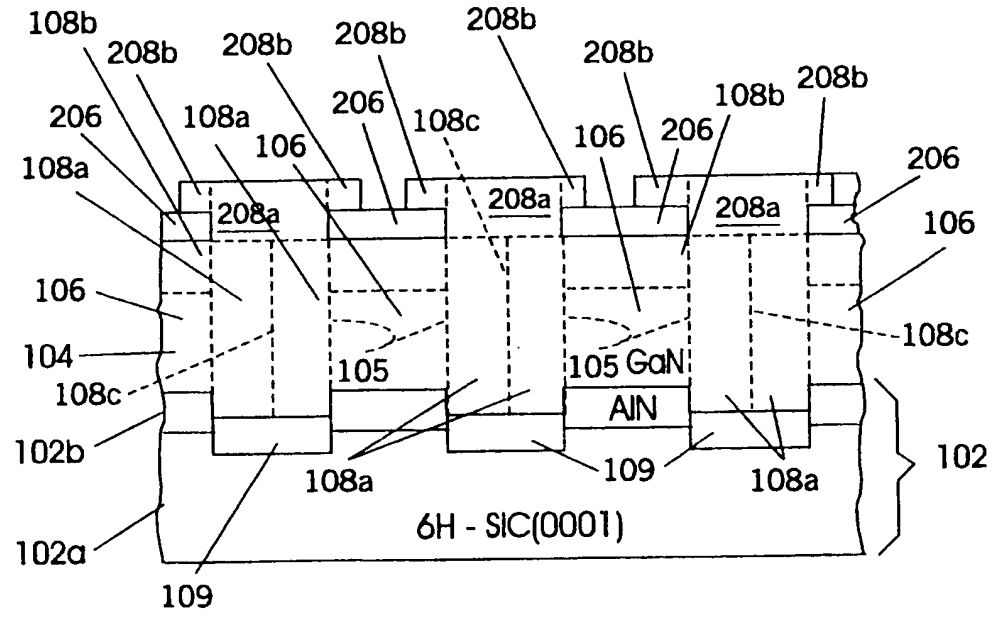
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FIG. 9

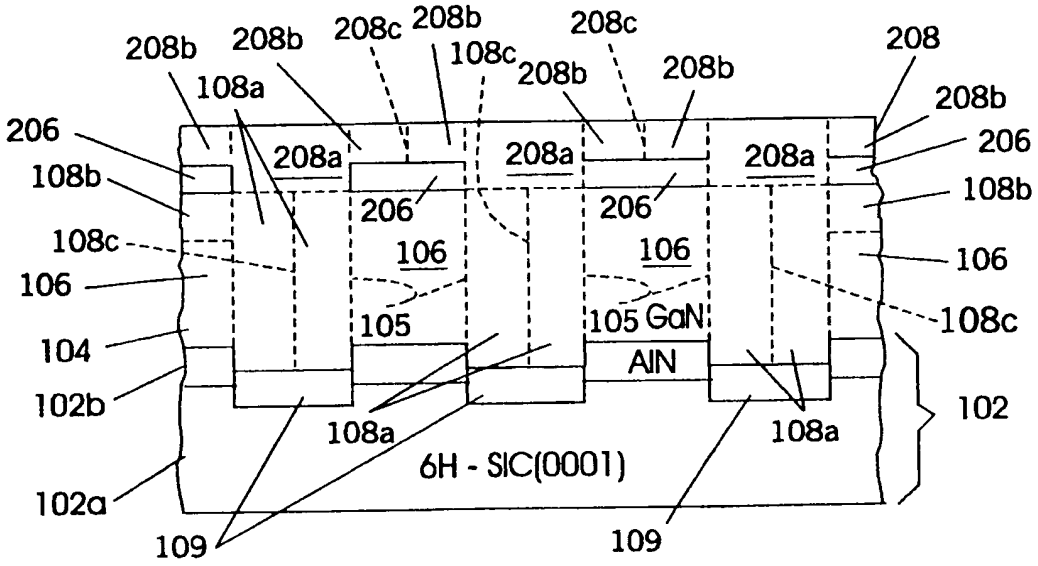
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FIG. 10

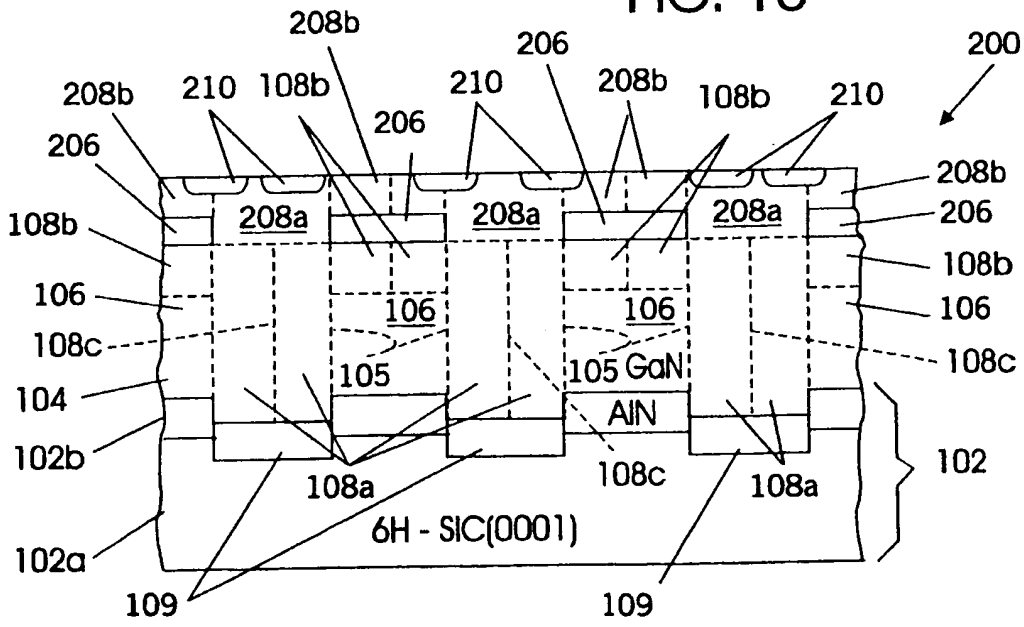
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FIG. 11

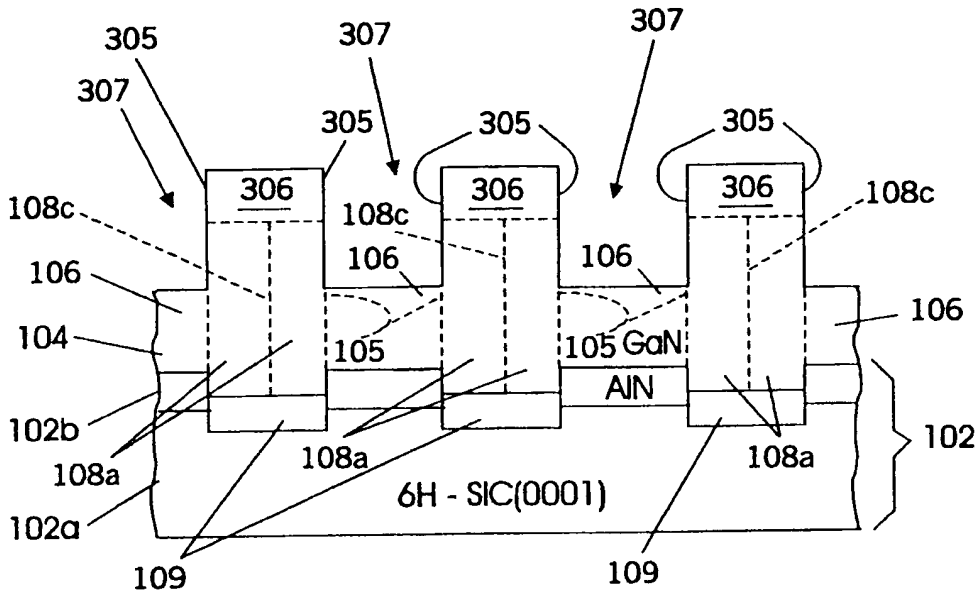
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FIG. 12

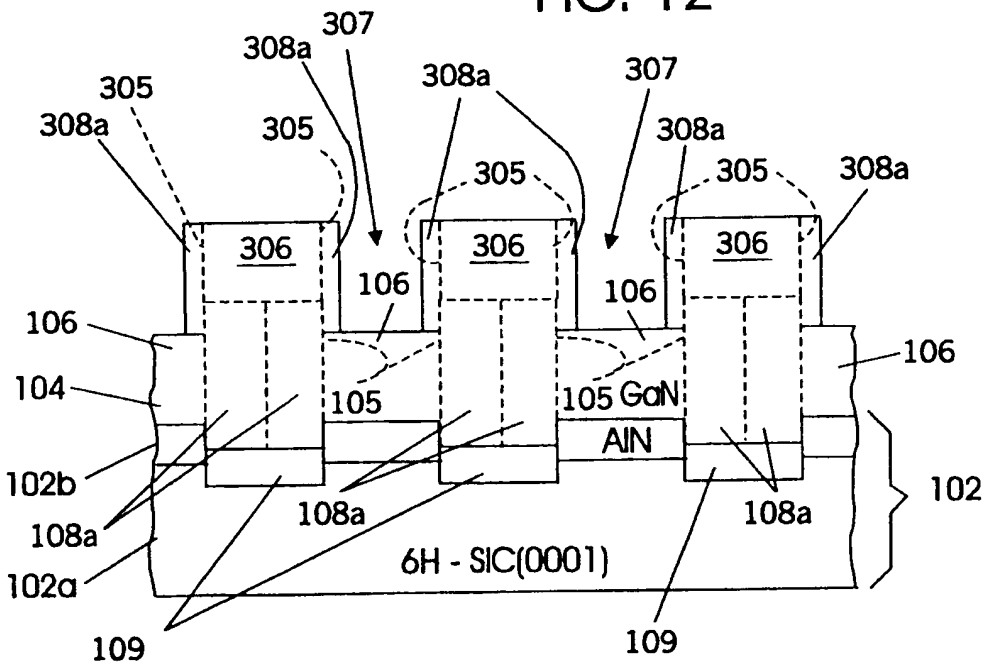
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FIG. 13

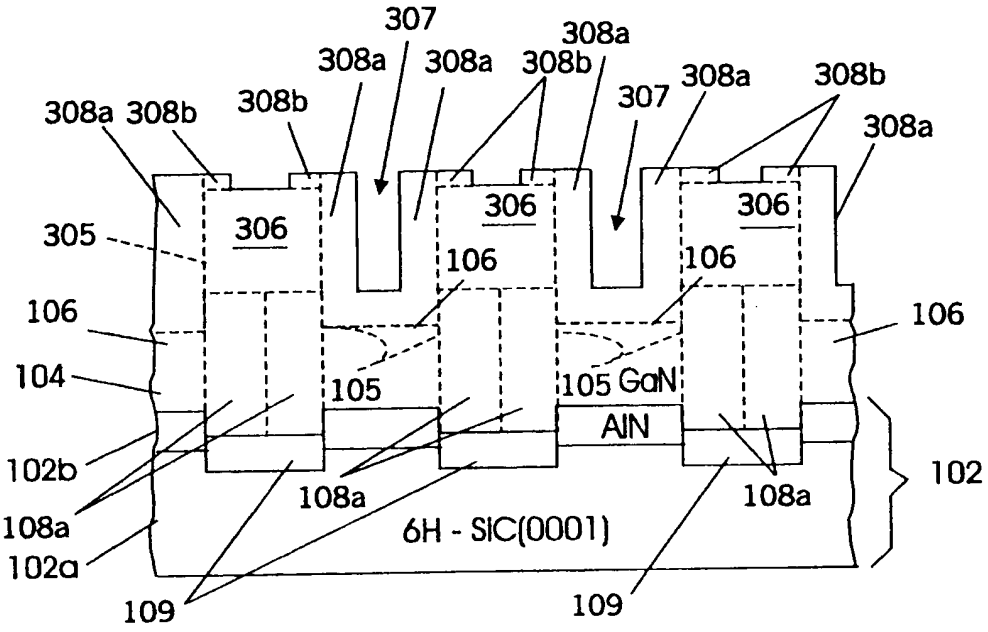
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FIG. 14

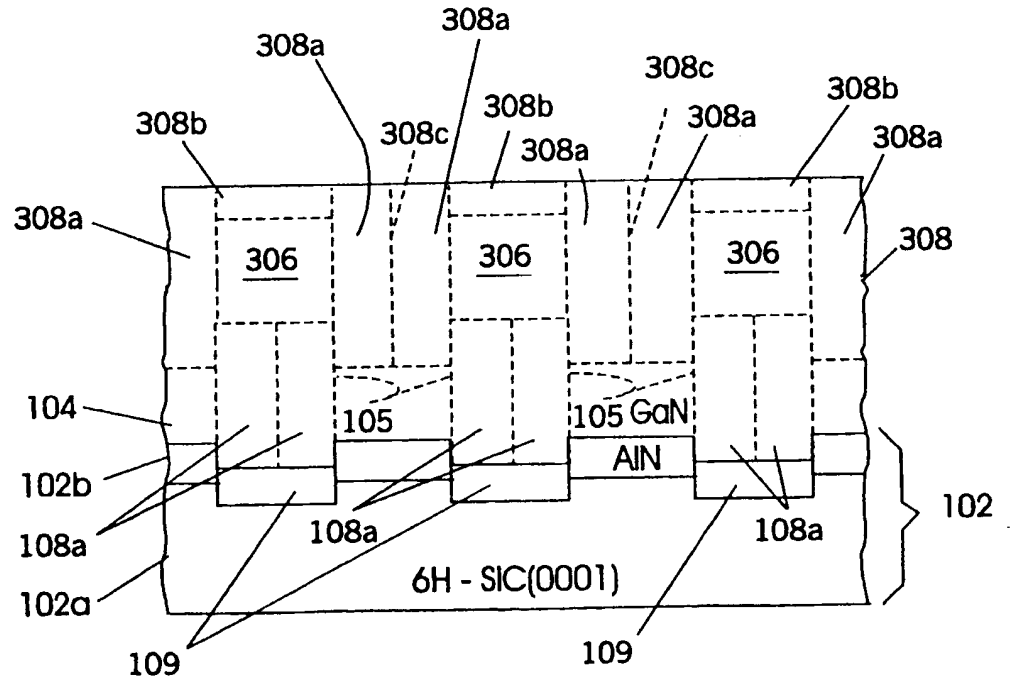
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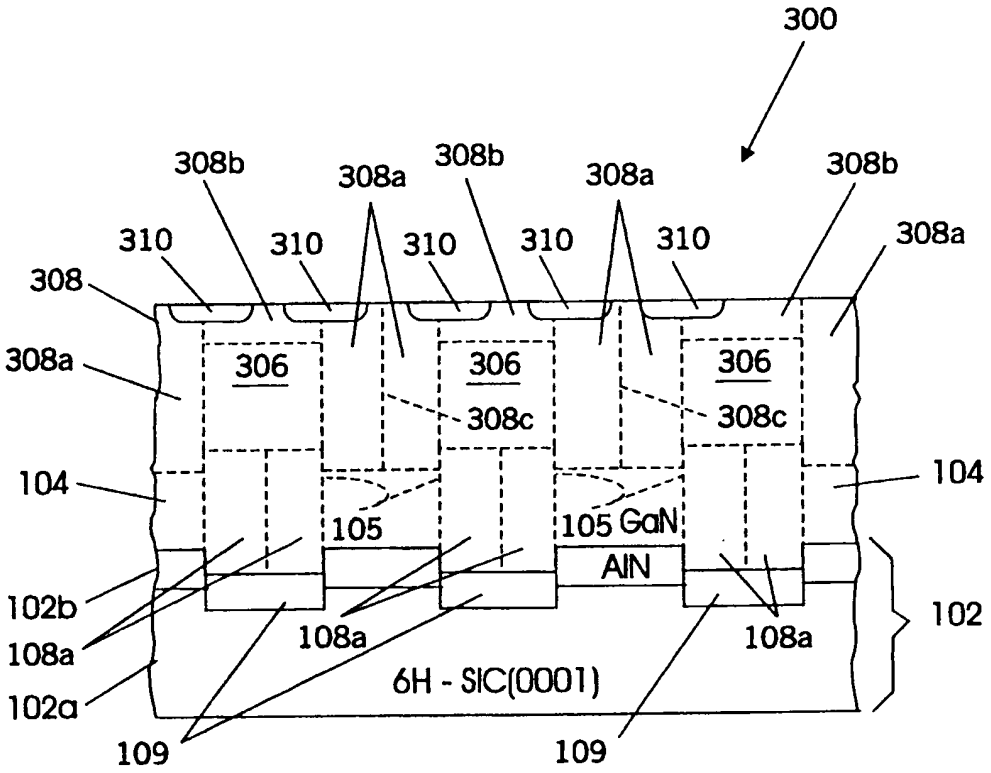
FIG. 15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INTERNATIONAL SEARCH REPORT

Int' tional Application No
PCT/US 99/12967

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/20 C30B25/04 C30B29/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L C30B C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 551 721 A (AMANO HIROSHI; AKASAKI ISAMU; PIONEER ELECTRONIC CORP; TOYODA GOSEI CO) 21 July 1993 (1993-07-21) page 4, line 32 -page 6, line 22; figure 4 -/--	1,3-5,7, 10,13, 14,16, 18,21, 26,29, 30,32, 35,36, 41,43

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 October 1999	18/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Köpf, C

3

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 99/12967

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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